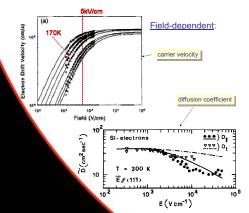


The LSST Sensor Development Program

V. Radeka (BNL), J. C. Geary (CfA), D. K. Gilmore (SLAC), M. Nordby (SLAC), J. A. Tyson (UC Davis), J. Oliver (Harvard), D. Figer (RIT), C. Stubbs (Harvard)

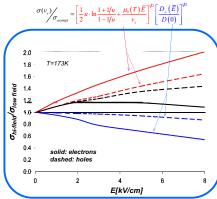
The LSST focal plane array (FPA) will consist of an order of magnitude more pixels than any imaging array realized so far. The sensors must produce low read noise, high QE at 1 micron, and a very tight PSF. This is driven by the LSST science. This poster describes the technical advances. For an FPA involving about 200 large format (4k x 4k) sensors, an industrial approach has to be developed and adopted. In this phase of sensor development, we have targeted specific technology experiments at selected vendors, with the goal of establishing both the technical characteristics of actual sensors, based on our projected requirements, and the industrial feasibility of their production. We have chosen to fund three projects in this development phase, two involving CCD technology and one utilizing hybridized PIN-CMOS architecture. Initial test results from the first devices in a smaller format resulting from this study program are encouraging.

Diffusion: Elementary Relations $\sigma = (2Dt)^{1/2}$ For $u \ge 2$, $[f(u)] \rightarrow 1$



ndent of the electric field?

Velocity Saturation Effect on Diffusion in Si



2. There is a decrease in the (transverse) diffusion coefficient due to the streamlining effect of the

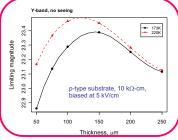
electric field on the carriers in random+drift

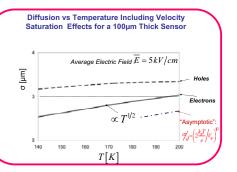
the diffusion due to a longer carrier drift time than expected in the constant mobility case;

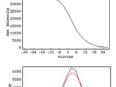
The two opposing effects result in an overall substrate sensors), and 1.3 for holes (n-substrate).



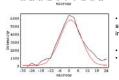
 1μ limiting mag. vs. thickness

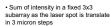












Differentiate the virtual knife edge.
 Fit to a Gaussian distribution.

Critical Technology Issues and R&D Status

Critical technology issues:

- Overdepleted thick sensor with independent
- Thin conductive (ohmic) window
- Segmented (multiport) readout
- Flatness

5. R&D under way:

Study contracts with two CCD vendors, to be completed by the first quarter of 2007, one study contract on PIN-CMOS. Prototype development to start in 2007.

Status of R&D and of the proofs of principle:

- Ilems 1, and 2, have been demonstrated by LBNL, MIT LL, e2v, JPL, and Hamamatsu.
- Segmented multiport readout has been demonstrated by several vendors. (This is a layout topology issue, and not a process technology issue as 1. and 2.)

- Successful (proprietary) methods for window processing have also been developed for thick overdepleted PIN-CMOS sensors by two vendors.

